

CLAIMS

1. A method of making a semiconductor package comprising:

providing a semiconductor chip carrier substrate having a first surface and a plurality of cavities formed in the first surface and wherein each cavity is defined, at least in part, by a bottom surface and at least one sidewall;

placing an integrated circuit chip, having bond pads on an upper surface thereof, in each of the cavities formed in the chip carrier substrate, and wherein each semiconductor chip overlies the bottom surface;

forming a first dielectric layer over the first surface of the chip carrier substrate and over the integrated circuit chip in each of the cavities.
2. A method as set forth in Claim 1 further comprising forming a first set of vias in the first dielectric layer and so that each of the first set of vias is aligned with a bond pad of the integrated circuit chip.
3. A method as set forth in Claim 2 further comprising forming an electrically conductive traces over the first dielectric layer and so that each one of the electrically conductive trace is electrically is connected to the one of the bond pads of the integrated circuit chip.

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4. A method as set forth in Claim 3 further comprising forming a second dielectric layer over the redistribution traces, and forming a second set of vias in the second dielectric layer so that each of the second set of vias communicates with one of the redistribution traces.

5. A method as set forth in Claim 4 further comprising forming electrically conductive bumps wherein each electrically conducted bump overlies the second dielectric layer and extends into one of the vias formed in the second dielectric layer and so that the electrically conductive bump is electrically connected to one of the redistribution traces.

6. A method as set forth in Claim 5 further comprising sectioning the semiconductor chip carrier into individual packages each including a semiconductor chip.

7. A method as set forth in Claim 1 wherein the semiconductor chip carrier comprises at least one of silicone, glass, ceramic, and plastic.

8. A method as set forth in Claim 1 wherein the plurality of cavities are formed by etching a semiconductor chip carrier substrate.

9. A method as set forth in Claim 1 wherein the cavities are formed by molding the semiconductor circuit chip carrier substrate to provide the cavities.

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10. A method as set forth in Claim 1 wherein the cavities are provided by milling a flat surface of a semiconductor chip carrier substrate.

11. A method as set forth in Claim 1 further comprising depositing an adhesive over the bottom surface defining each cavity prior to placing the integrated circuit chip in each cavity.

12. A method as set forth in Claim 2 wherein the first set of vias formed in the first dielectric layer are formed by reactive ion etching.

13. A method as set forth in Claim 1 wherein the first dielectric layer comprises at least one of a polyimide and BCB.

14. A method as set forth in Claim 3 wherein the electrically conductive redistribution traces comprise copper.

15. A method as set forth in Claim 14 wherein the electrically conductive redistribution traces further comprise nickel.

16. A method as set forth in Claim 4 wherein the second dielectric layer comprises at least one of a polyimide and BCB.

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17. A method as set forth in Claim 4 wherein the second set of vias is formed in the second dielectric layer by reactive ion etching.

18. A method as set forth in Claim 5 wherein the electrically conductive bumps are formed by at least one of ball placement, stenciling, and plating.

19. A method as set forth in Claim 6 wherein the sectioning comprises cutting the chip carrier substrate with a saw.

20. A method of making a semiconductor package comprising:

providing a wafer size semiconductor chip carrier substrate having a first surface and a plurality of cavities formed in the first surface and wherein each cavity is defined, at least in part, by a bottom surface and at least one sidewall;

placing an integrated circuit chip, having bond pads on an upper surface thereof, in each of the cavities formed in the wafer size chip carrier substrate, and wherein each semiconductor chip overlies the bottom surface;

forming a first dielectric layer over the first surface of the chip carrier substrate and over the integrated circuit chip in each of the cavities;

forming a first set of vias in the first dielectric layer and so that each of the first set of vias is aligned with a bond pad of the integrated circuit chip;

forming an electrically conductive layer over the first dielectric layer and down into the vias formed in the first dielectric layer and selectively removing portions of the

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electrically conductive layer to form electrically conductive traces and so that each one of the electrically conductive trace is electrically is connected to the one of the bond pads of the integrated circuit chip;

forming a second dielectric layer over the redistribution traces, and forming a second set of vias in the second dielectric layer so that each vias communicates with one of the redistribution traces;

forming electrically conductive bumps wherein each electrically conducted bump overlies the second dielectric layer and extends into one of the vias formed in the second dielectric layer and so that the electrically conductive bump is electrically connected to one of the redistribution traces;

sectioning the semiconductor chip carrier so into individual packages each including a semiconductor chip.

21. A method as set forth in Claim 20 wherein the semiconductor chip carrier comprises at least one of silicone, glass, ceramic, and plastic.

22. A method as set forth in Claim 20 wherein the plurality of cavities are formed by etching a semiconductor chip carrier substrate.

23. A method as set forth in Claim 20 wherein the cavities are formed by molding the semiconductor circuit chip carrier substrate to provide the cavities.

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24. A method as set forth in Claim 20 wherein the cavities are provided by milling a flat surface of a semiconductor chip carrier substrate.

25. A method as set forth in Claim 20 further comprising depositing an adhesive over the bottom surface defining each cavity prior to placing the integrated circuit chip in each cavity.

26. A method as set forth in Claim 21 wherein the first set of vias formed in the first dielectric layer are formed by reactive ion etching.

27. A method as set forth in Claim 20 wherein the first dielectric layer comprises at least one of a polyimide and BCB.

28. A method as set forth in Claim 20 wherein the electrically conductive redistribution traces comprise copper.

29. A method as set forth in Claim 28 wherein the electrically conductive redistribution traces further comprise nickel.

30. A method as set forth in Claim 20 wherein the second dielectric layer comprises at least one of a polyimide and BCB.

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31. A method as set forth in Claim 20 wherein the second set of vias is formed in the second dielectric layer by reactive ion etching.

32. A method as set forth in Claim 20 wherein the electrically conductive bumps are formed by at least one of ball placement, printing, and plating.

33. A method as set forth in Claim 20 wherein the sectioning comprises cutting the chip carrier substrate with a saw.

34. A semiconductor package comprising:

- a semiconductor chip carrier substrate having a first surface and a plurality of cavities formed in the first surface and wherein each cavity is defined, at least in part, by a bottom surface and at least one sidewall;
- an integrated circuit chip, having bond pads on an upper surface thereof, in each of the cavities formed in the chip carrier substrate, and wherein each semiconductor chip overlies the bottom surface;
- a first dielectric layer over the first surface of the chip carrier substrate and over the integrated circuit chip in each of the cavities;
- a first set of vias in the first dielectric layer and so that each via is aligned with a bond pad of the integrated circuit chip;
- an electrically conductive traces over the first dielectric layer and one of the traces extending down into the one of the vias formed in the first dielectric layer so that each one of the

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electrically conductive trace is electrically connected to the one of the bond pads of the integrated circuit chip;

a second dielectric layer over the redistribution traces, and a second set of vias in the second dielectric layer so that each vias communicates with one of the redistribution traces;

electrically conductive bumps wherein each electrically conducted bump overlies the second dielectric layer and extends into one of the vias formed in the second dielectric layer and so that the electrically conductive bump is electrically connected to one of the redistribution traces.

35. A semiconductor package as set forth in Claim 34 wherein the semiconductor chip carrier comprises at least one of silicone, glass, ceramic, and plastic.

36. A semiconductor package as set forth in Claim 34 further comprising an adhesive over the bottom surface defining each cavity and underlying the integrated circuit chip in each cavity.

37. A semiconductor package as set forth in Claim 34 wherein the first dielectric layer comprises at least one of a polyimide and BCB.

38. A semiconductor package as set forth in Claim 34 wherein the electrically conductive redistribution traces comprise copper.

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40. A semiconductor package as set forth in Claim 38 wherein the electrically conductive redistribution traces further comprise nickel.

41. A semiconductor package as set forth in Claim 34 wherein the second dielectric layer comprises at least one of a polyimide and BCB.